"Hierarchical CAD Tools for Radiation Hardened Mixed Signal Electronic Circuits"

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Silvaco Data Systems
Dr. Christopher Nicklaw
Principal Investigator
4701 Patrick Henry Drive
Building #2
Santa Clara, CA 95054
408-654-4303

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Hierarchical CAD Tools for Radiation Hardened Mixed Signal Electronic Circuits

Silvaco Data Systems
Christopher Nicklaw
Mark Maurer

Peregrine Semiconductor
Jim Swonger
Chuck Tabbert

The Titan Corporation
Randall Milanowski
Marion Rose
Joseph Azarewicz

28 January 2005

Prepared for:

Defense Advanced Research Projects Agency (DARPA)
ATTN: MTO (Dr. Anantha Krishnan, Sponsor)
3701 North Fairfax Drive
Arlington, VA 22203-1714

Defense Advanced Research Projects Agency (DARPA)
ATTN: MTO (Riva Meade, ADPM)
3701 North Fairfax Drive
Arlington VA, 22203-1714

U.S. Army Aviation and Missile Command
ATTN: AMSRD-AMR-WS-DP-SB (Barry Lineberry, Technical Monitor)
Bldg 7804, Room 222
Redstone Arsenal, AL 35898

Under Contract:
W31P4Q-04-C-R2776

Prepared by:
Silvaco Data Systems
4701 Patrick Henry Drive
Santa Clara, CA 95054

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EXECUTIVE SUMMARY

Through out our efforts during this Phase I DARPA contract, our team was faced with three core challenges impeding the development of robust solutions to the lack of Electronic Design Automation (EDA) tools for radiation aware design.

- The first being a lack of a commercially available Analog Mixed-Signal (AMS) circuit simulator, which understood radiation effects.
- Secondly the absence of a mechanism to verify the simulation results
- Finally the design methodology to utilize this new capability had to be developed with an eye towards integration into existing design flows for both tool and systems engineering compatibility.

Knowing from the day we submitted our proposal to DARPA these challenges would face us we set out to assemble an industry team of acknowledged experts. Unique capabilities were required in software development, the design of military electronics operating in radiation environments, and systems engineering. To this end Silvaco Data Systems is a leading provider of commercial EDA software with a history of making modifications to suit specialized military needs. Peregrine Semiconductor is a renowned supplier of high performance military electronics with both integrated circuit (IC) design, and manufacturing experience. The Titan Corporation's (branch formerly known as Jaycor) has a legacy of systems engineering and qualification for military systems.

The goal of this effort was the specification, development, and deployment of an integrated suite of software tools enabling radiation aware mixed signal design. At the heart of any mixed signal design flow is the circuit simulator- and this is where we focused our attention modifying the Silvaco Harmony-AMS package to enable the simulation of Single Event Effects (SEE), Dose Rate (DR), Total Ionizing Dose (TID), and combined environments

The technical report which follows details the results of our collaboration and we are more than willing to answer any questions you may have after your review of our efforts.

Mark Maurer
Manager, Government Business Division
Silvaco Data Systems
4701 Patrick Henry Drive
Santa Clara, CA 95054
408-654-4303 phone
mark.maurer@silvaco.com

1.0 BACKGROUND

Commercial mixed signal simulators enable the creation of System on a Chip (SOC) designs, which require understanding the interface of analog and digital circuitry. Combining the analog and digital elements onto a single chip has several advantages, but also creates unique challenges for both designers and simulators. To accomplish this goal a simulator must have the capability to model the analog portion of the chip in an analog simulation language such as (**S**imulation **P**rogram with **I**ntegrated **C**ircuit **E**mphasis) SPICE language, and the digital elements in a digital language. Silvaco's product SmartSpice has been a pure analog simulator since it's introduction in 1987 and is one of the leading SPICE simulators available today. SmartSpice utilizes the original syntax structure established at the University of California Berkeley and is compatible with HSPICE and PSPICE, which are two other widely used commercial simulators. The SPICE language has been the gold standard for analog designers for decades and the models developed for the engine have been continually updated to simulate the most advanced technology.

The digital languages have been a much more difficult target to track than SPICE. There have been several major Hardware Design Languages (HDL) standards over the years the most notable VHDL, Verilog, and countless varieties of each to complicate matters. The IEEE has made efforts to standardize the languages to simplify their utilization for commercial use, but even at the time of this report on-going battles over the 'standard' continue. The decision between Verilog and VHDL has been made in the commercial world with the United States and Asia supporting Verilog, leaving VHDL in Europe, university environments, and legacy military design.

Much of the commercial EDA industry has adopted IEEE-1364 Verilog HDL as the industry standard, and will update their language support as the various standards committees make their final recommendations. Silvaco, like much of the commercial EDA industry, has standardized on IEEE 1364-2001 for Verilog-D and Verilog-AMS from Accellera. Verilog-AMS is a modeling language for mixed signal (analog and digital signals) systems supporting the description of both digital and analog components. Verilog-AMS is the merger of Verilog-HDL (IEEE –1364-2001) and Verilog-A. Verilog-AMS is under the control of Accellera which is an independent organization dedicated to the improvement of language based design automation. This set of languages provide the maximum support for interoperability between Silvaco and other EDA toolsets for digital functions such as synthesis, place and route, and full chip timing and parasitic extraction.

1.1 MIXED SIGNAL TECHNICAL INTRODUCTION

Mixed-signal designs are becoming more frequent and complex with very short time-to-market windows. Portable, low power wireless electronic products are driving mixed signal designs and these circuits are very complex. Current cell phone's can contain over 10 million transistors. Mixed-signal chips implement complex algorithms that require designers to examine their operation over thousands of cycles, such as Phase Lock Loops, delta-sigma converters, and spread spectrum transceivers. System circuit complexity is increasing at a rate that is outpacing designers' ability to keep up. A top-down engineering process based on an iterative, hierarchical implementation of system requirements supporting trade studies must be utilized. This top-down design process allows for an incremental and methodical approach for transforming the design from an abstract block diagram of system requirements to a detailed transistor-level implementation.

This top-down approach is common in most Department of Defense contractors as it is the very basis of System Engineering. System Engineering is responsible for verifying that the system developed meets all requirements defined in the system specification, and for providing the complete analysis to assure that all requirements will be met. The commercial market place has recognized the benefits of this top down design process and is rapidly adopting these practices. It has been most prevalent in the digital electronics design process with the use of Hardware Descriptive Languages (HDL's) of Verilog-D (IEEE-1364) and VHDL (IEEE –1076). These HDL's have allowed digital designers the capability to manage complexity and size of digital systems that now exceed 100's of millions of transistors.

1.2 BOTTOM-UP VS. TOP-DOWN DESIGN

The established approach to design is known as bottom-up design. The design process starts with the design of the individual blocks, which are then combined to form the system. The design of the blocks starts with a set of specifications and ends with a transistor level implementation. Each block is verified as a stand-alone unit against specifications and not in the framework of the overall system. Once verified individually, the blocks are then combined and verified together, but at this point the entire system is represented at the transistor level. The bottom-up design style is effective for small designs, but often fails in complex and large designs due to communication problems. Here we see one of the main benefits of Mixed Signal Simulation: It extends the top-down approach farther down into the highly optimization dependent analog parts of a SoC. Now bring radiation-effects into the picture: *making mixed signal simulation radiation-aware provides an unprecedented means for radiation hardened system design to also be a top-down process*: It provides a path from system requirements specifications all the way down to physical radiation response at the transistor level.

A top-down design process systematically proceeds from architecture- to transistor-level design. Each level is fully designed before proceeding to the next and each level is fully leveraged in design of the next. It acts to partition the design into smaller, well-defined blocks, and allowing more designers to work together productively.

The center of a top-down design methodology is the comprehensive simulation plan, which in turn leads to a modeling plan. The process begins by identifying particular areas of concern in the design. Plans are then developed for how each area of concern will be explored and verified. The plans specify how the tests are preformed, and which blocks are at the transistor level during the test. For example, if an area of concern is the loading of one block on another, the plan might specify that one test should include both blocks represented at the transistor level together. For those blocks for which models are used, the effects required to be included in the model are identified for each test. This is the beginning the modeling plan. Typically, many different models will be created for each block. These models may be written either by the circuit or system architect or the block designer.

1.3 DIGITAL DESIGN

The digital designer of today uses a top-down design and a bottom-up verification methodology. HDL's support executable specification development through simulation and synthesis. Simulation allows the application of stimuli to the executable model described by the HDL, allowing the designer to examine its response. Simulation supports the designer's understanding of the design before incurring the cost of implementing the design. Synthesis is the process of actually implementing the executable model in hardware. The HDL describes the design at an abstract level using constructs to develop a model that does not yet have a physical (transistor level) implementation. Synthesis refines this abstract description with equivalent behavior at the inputs and outputs with components that have a physical implementation. Synthesis converts a well-defined subset of an HDL often referred to as register-transfer level (RTL) to an optimized gate level description. These gate level implementations are available in the library of standard cells generally provided / supported by the foundry.

Verification of digital designs done with HDL's is accomplished using SPICE or a SPICE like simulator. SPICE like simulator allow for approximations of behavior and hierarchical approaches to simulation. The trade gives up accuracy for speed, complexity and size of circuitry.

1.4 ANALOG DESIGN

Analog design continues to be at the device (transistor and diode) and component (capacitor, resistor, and inductor) level utilizing SPICE to simulate the

interconnected devices and components behavior under an applied stimulus. Analog signals are signals that vary continuously. The value of the signal, at any point, may take on any value within a continuous range of values. This varies from digital design in that the digital signals usually have only two possible values high (one or high supply or low (zero or ground). The analog designer is aware of the circuits operating point, its DC and AC characteristics. Automated synthesis of an Analog or Mixed Signal system from a description of its behavior is not at a state similar to the digital domain.

Digital synthesis maps digital behavior onto digital gates that are arranged in a rather constrained topology. Logic gates combined with the constrained topology makes synthesis feasible. The analog building blocks are much more complex and varied and the topology is completely unconstrained. These issues make analog synthesis amore difficult problem than digital synthesis. Without analog synthesis, analog design is done the old fashioned way, with designers manually converting specifications to circuits. While this allows for more creativity, it also results in more errors, particularly those that stem from communication errors. These miscommunications prevent the system from operating properly when the blocks are assembled even though the blocks were thought to be correct when tested individually.

There has been progress in the analog and mixed signal (digital and analog signals) design with the aid of analog behavioral language support. Today both Verilog-AMS and VHDL-AMS provide analog behavioral modeling capability. Behavioral modeling represents behavior of a device rather than mimicking its actual implementation. The models can be implemented at several different levels from a simple op amp to a complex multi-pole/zero op amp. Most recent developments within the analog behavioral modeling capabilities is the constructs for describing transistor behavior with such constructs as integral, derivative and limiting exponential functions. These extensions for transistor modeling is supported by the Compact Modeling Councils (CMC) mandate that the next generation compact models be submitted for approval using Verilog-AMS 2.2.

2.0 TECHNICAL APPROACH FOR MIXED SIGNAL with RADIATION

Our team's technical approach was to integrate two commercial tools; a Verilog simulator compliant to Verilog-1364-2001 and a SPICE simulator. This integration would be compliant to the Verilog-AMS standard from Accellera.

An Analog Mixed Signal (AMS) parser allocates digital logic to be simulated under the Verilog simulator, while all analog portions would be simulated under SPICE. A Timing Manager Module (TMM) coordinates timing issues. This means that analog time points are coordinated to match digital events. This allows the analog portion to use various algorithmic schemes to resolve convergence issues within the analog portion of the mixed signal system.

In the initial technology characterization phase, radiation issues are simulated in the analog domain due to radiation being a time continuous event. This is supported within the Verilog-AMS standard in that any block within a Mixed Signal design can itself be Mixed Signal, analog or digital (see Figure 1). Once analog-domain radiation effects simulations have determined the radiation response behavior for sub circuits and circuits, one can construct radiation behavioral models for blocks to be used at the system level to understand system level radiation response and any digital block or portion of any digital block can be represented at the transistor level and its radiation response examined within a Mixed Signal simulation.

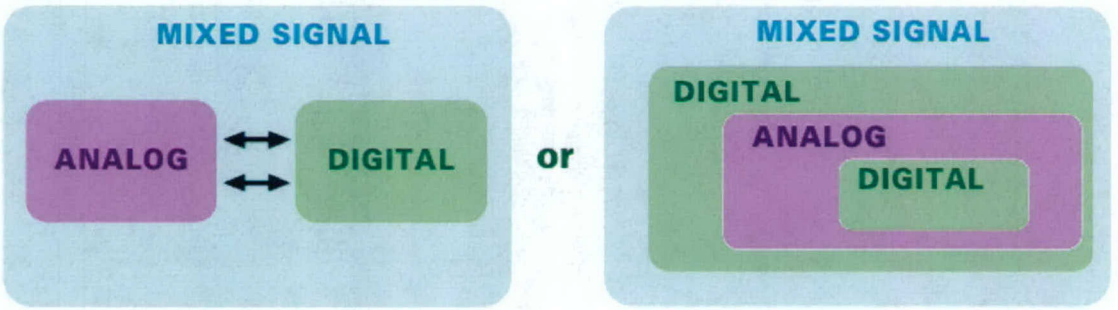

Figure 1: Mixed Signal System Make-Up.

2.1 TECHNICAL CHALLENGE

The time control algorithm that coordinates timing issues of a SPICE simulator with radiation analysis capability and a digital simulator. This fundamental numerical methods challenge exists in standard mixed signal simulation; adding radiation effects to the SPICE side, and still maintaining a working integrated tool has never been shown prior to this effort.

2.2 HIGH PAY-OFF

A standards-compliant, commercially accepted Mixed Signal simulator, supporting radiation analysis as yet another specification requirement. The reason commercial acceptance is important for a tool is because it connects an advanced simulation capability to the modern manufacturing base. The DoD design community, those responsible for delivering parts for future systems, must use tool flows that are supported by available foundries. Our objective is a tool that allows Radiation Hardening By Design (RHBD) to be applied in the modern fabless model and to provide tool support to allow RHBD to be deployed in the DoD design community at large.

2.3 MIXED SIGNAL SIMULATION with RADIATION

The addition of the capability to model radiation events inside of Harmony-AMS, Mixed Signal simulator (see Figure 2), is based on the integration SmartSpice RadHard, a SPICE based analog simulator, in which radiation circuit models were developed for SEE, and Dose Rate (DR), and Total Ionizing Dose (TID). This development was funded internally by Silvaco and as been a successful proof of concept for the executive management at Silvaco. We limited our costs to a great degree by taking the same source code developed for the commercial simulator and adding only the features and physics required for the defined specification for the RadHard module. This approach allowed all of the benefits of the commercially supported SmartSpice (foundry issued SPICE models, latest updated models, large development and applications engineering staff) to be leveraged by military electronics designers. The cost structure associated with a specialized add-on module to an exciting product; facilitates a business model in which specialized software can be developed and deployed for specific military needs such as Hardening by Design (HBD).

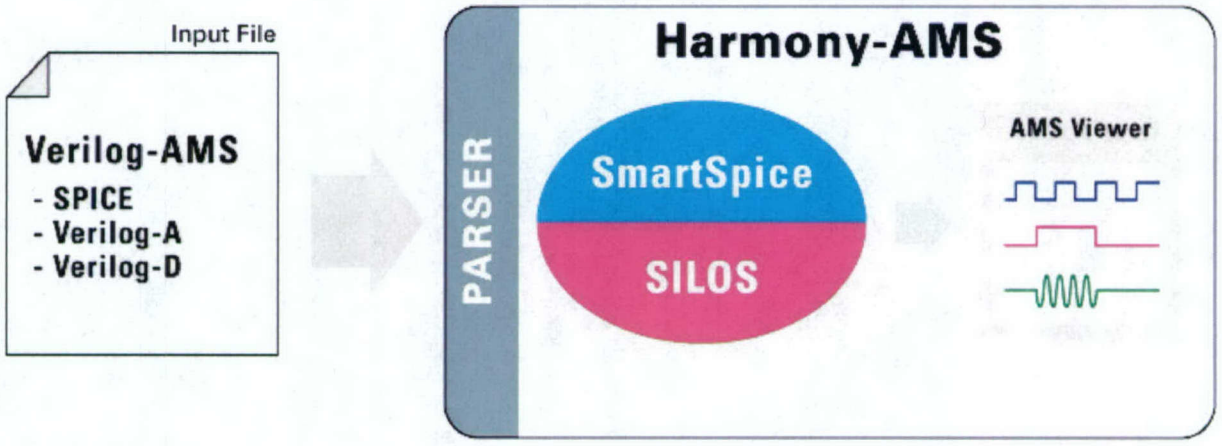

Figure 2: Harmony-AMS Analog/Mixed Signal Simulator with integrated viewer

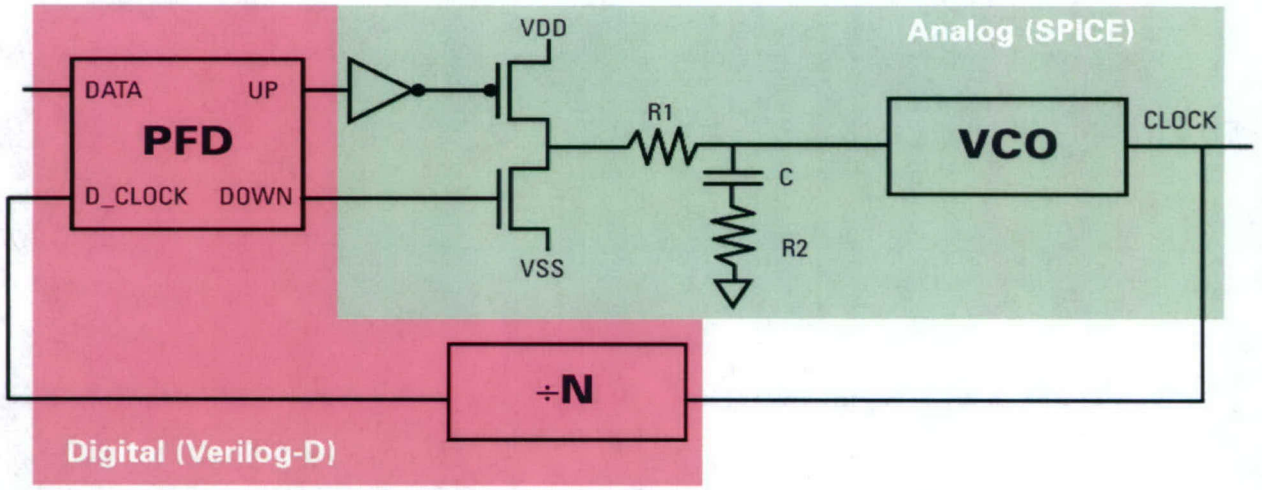

Figure 3: Schematic representation of digital and analog elements

3.0 SOFTWARE DEVELOPMENT

Our approach to the Radiation Hardened Mixed Signal Electronic Circuits program was similar in scope to our internal development of SmartSpice RadHard. We started with the commercial Harmony-AMS product and identified the additional work required to enhance the tools capability to include radiation modeling. The major difference being the funding provided by DARPA, which made it possible. . This funding allowed the development of significant and unique enhancements to the Timing Manager module so it could coordinate digital events with radiation continuum time domain of SmartSpice RadHard.

One of the lessons SILVACO has learned during its ~15 year experience supporting DoD radiation hardened electronics is that it is critical to involve experienced end users as early as possible during the development of the tool. It is the "easy way out" to develop software in a vacuum with out customer criticism during the early stages; however the product will suffer later from the lack of tough criticism during development. This is true of all software but particularly in the case of specialized code for the military community as our developers are experienced in software development not radiation hardened circuit design.

This experience factored into the selection of our team members when we assembled the team for this proposal. Peregrine Semiconductor is a leading design and manufacturing contractor for radiation hardened military electronics. The Titan Corporation, specifically the former Jaycor office in San Diego, has vast experience in systems level integration, testing, and specification

requirements for military systems. The combination of this expertise allowed the software developers at Silvaco to tap into the experience of our partners to create a more complete product that may have been possible otherwise.

Harmony-AMS provided an excellent starting point as it integrated mature products (SmartSpice & Silos) with the SmartSpice simulator having the capability to read in both SPICE and Verilog-A. The development team used the C++ language and ensured that the product would operate on Windows 2000/XP, Linux RedHat 7.x, 9.x, and Enterprise 3, and Sun Solaris 8 and 9. The development team decided to support a 64-bit version of Harmony-AMS. The key advantage of the 64-bit software is the additional simulation capacity allowed by the improved memory architectures of the chips, chip sets, and motherboards.

Besides modeling nominal device behavior, modeling space microelectronics requires the ability to explore designs capable of operation in a radiation environment. The capability for radiation effects modeling within Harmony-AMS to date has been examined on three fronts, analog, digital and mixed signal. Figure 3. Provides a schematic overview of a Phase Lock Loop our Team use to valid the effects of an ion strike.

3.1 INPUT & CONTROL STATEMENTS

Analog modeling of radiation events such as TID, SEE, and DR, was accomplished by the implementation of radiation SPICE behavioral primitives that support the capability of Radiation Macro-models, the implementation of Verilog-AMS within our SPICE simulator, and finally through the implementation of radiation device models for BSIM3/4, MEXTRAM and VBIC BJT. These models are added to our SPICE tool, SmartSpice, as a dynamically linked library (.dll) files. Silvaco has extended the SPICE **.TRAN** statement to support SEE, TID, and DR analysis. The extension to the **.TRAN** statement for SEE supports the movement of the ion strikes throughout the circuit (see Figures 4 & 5). The implementation of Compact Modeling capability within Verilog-AMS allows a very powerful method of modeling radiation effects on microelectronics and the ability to exchange these models with other EDA tools. Silvaco has been and continues to be involved in Compact Modeling extensions committee for Verilog-AMS ensuring that the needed constructs for advanced modeling are incorporated within the Accellera Verilog-AMS standard.

DOSE RATE SYNTAX

```
.TRAN tstep tstop <tstart> <tmax> <UIC>
+ <CALLV> <SAVEV < =tsave>> <TRANOP < =top>> <STORE=num> <sw2_spcf>
+ <DR> <DOSERATE=val>
+ <START=val> <WIDTH=val>
+ <TAUN=val> <TAUP=val> <LN=val> <LP=val>
+ <NA=val> <ND=val>
```

DR: causes SmartSpice to perform a radiation analysis during simulation

DOSERATE: dose rate value (rad/s) (use if RAD=1 only).

START: start time of radiation pulse (s) (used for Wirth & Rogers)

WIDTH: start time of radiation pulse (s) (used for Wirth & Rogers)

TAUN: electron minority carrier lifetime in p-type (by default, 200ns) (used for Wirth & Rogers).

TAUP: hole minoirty carrier lifetime in n-type (by default, 200ns) (used for Wirth & Rogers)

LN: electron diffusion lenght (by default, 600μm) (used for Wirth & Rogers)

LP: hole diffusion lenght (by default, 300μm) (used for Wirth & Rogers)

NA: doping concentration (by default, 1E+17 at./cm^3) (used for diode models)

ND: doping concentration (by default, 1E+17 at./cm^3) (used for diode models)

Figure 4: Dose Rate Syntax

SEE SYNTAX FORM 1

```
.TRAN tstep tstop <tstart> <tmax> <UIC>
+ <CALLV> <SAVEV < =tsave>> <TRANOP < =top>> <STORE=num> <sw2_spcf>
+ <SEE> <START=val>
+ <DEVICE=string> <NODE=string> <ISEU=val>
```

SEE: Causes SmartSpice to perform a radiation analysis during simulation.

START: time of the impact.

TAUF: Collection time-constant of the junction

TAUR: Ion-trak establishment time constant.

DEVICE: device impacted by heavy ion.

NODE: Intrinsic node of the device impacted by the heavy ion (default node: drain).

ISEU: Maximun current (A).

SEE SYNTAX FORM 2

```
.TRAN tstep tstop <tstart> <tmax> <UIC>
+ <CALLV> <SAVEV < =tsave>> <TRANOP < =top>> <STORE=num> <sw2_spcf>
+ <SEE> <START=val>
+ <DEVICE=string> <NODE=string> <LF=val> <LET=val>
```

SEE: Causes SmartSpice to perform a radiation analysis during simulation.

START: time of the impact.

TAUF: Collection time-constant of the junction.

TAUR: Ion-trak establishment time constant.

DEVICE: device impacted by heavy ion.

NODE: Intrinsic node of the device impacted by the heavy ion (default node: drain).

LF: Particle funnel length (m).

LET: Linear Energy Transfer (Mev.mg/cm^2).

Figure 5: SEE Syntax

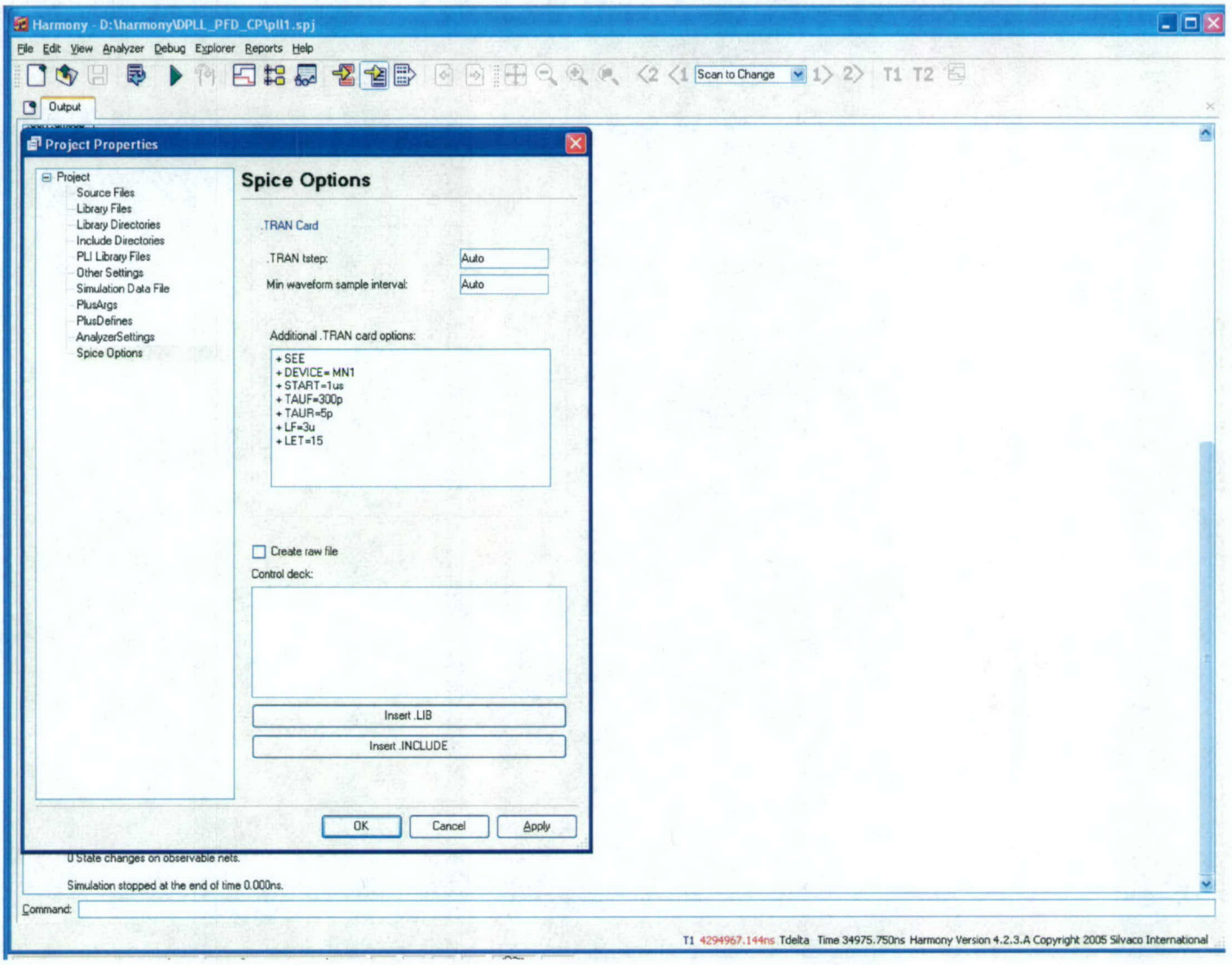

Figure 6: SPICE OPTIONS for SEE analysis within Harmony-AMS using the underlying syntax described in Figures 3 and 4

3.2 COMPACT MODELING FRAMEWORK for RADIATOIN EFFECTS

The basic EDA mechanisms for implementation of macro-models and Verilog-AMS can be developed and explored using Compact Modeling Framework for Radiation Effects. This framework allows the engineer to develop and analyze radiation modeling before incorporating it into the Harmony-AMS mixed signal environment.

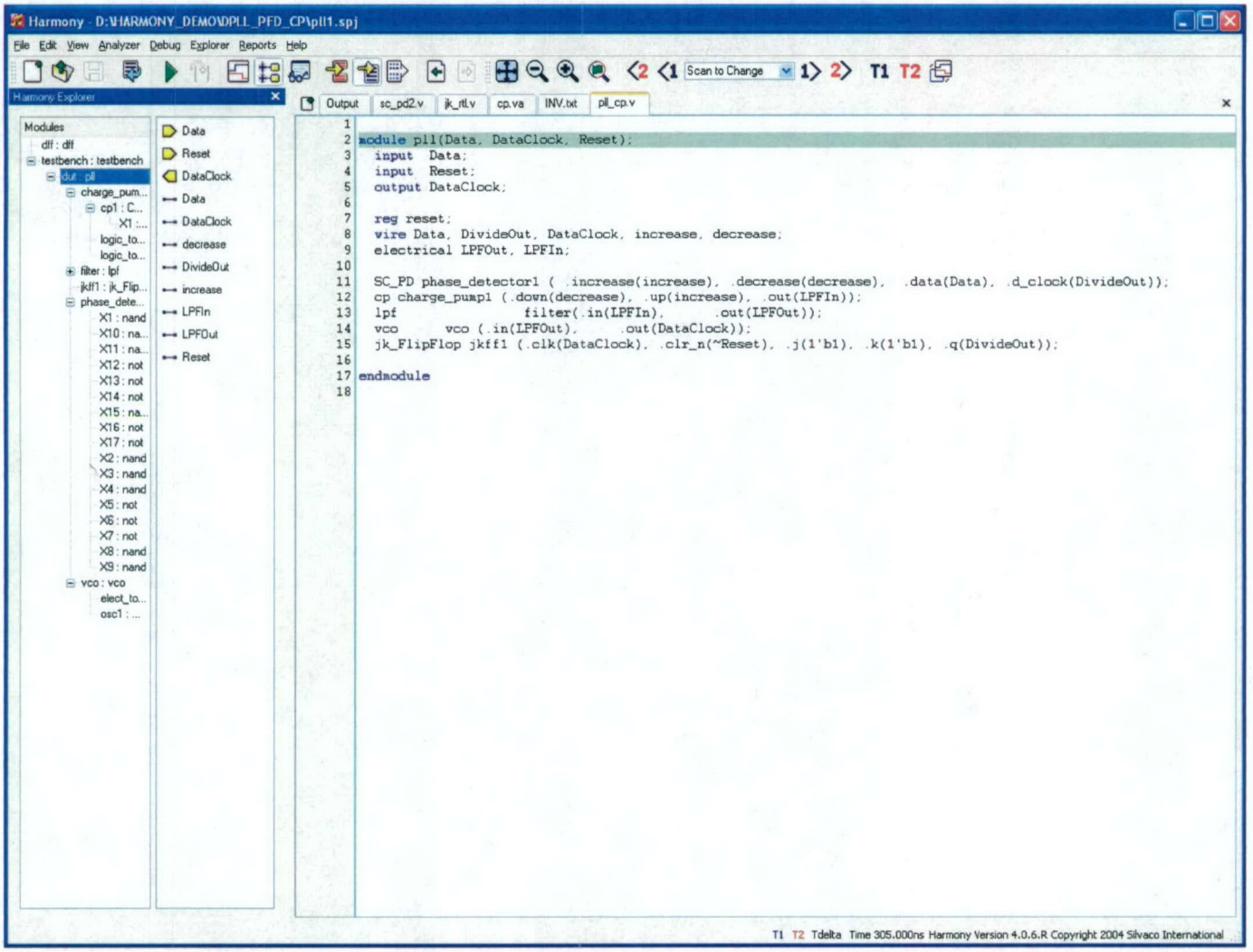

Figure 7: Compact Model Development Environment that supports the development and analysis of models that support radiation effects

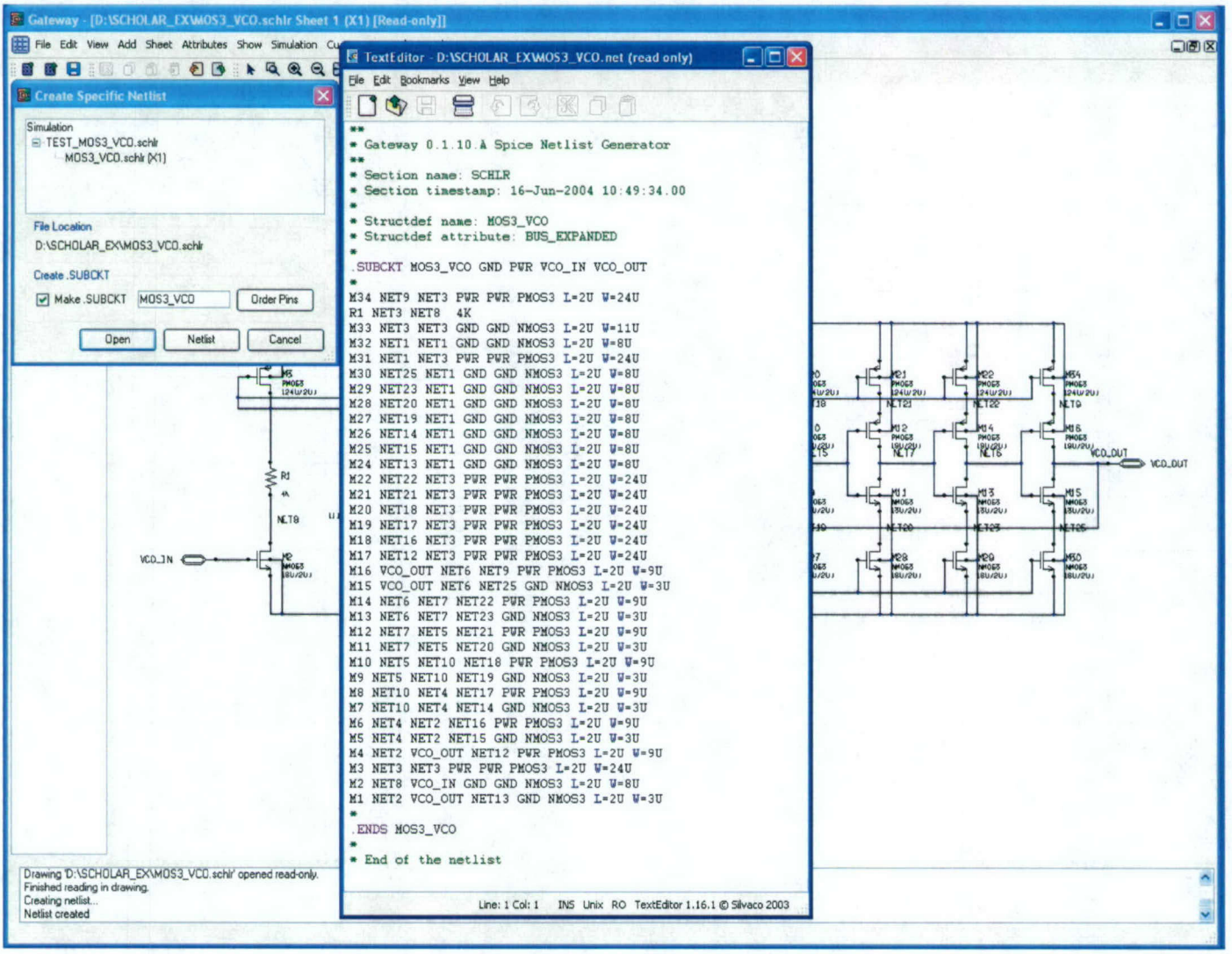

Figure 8: Gateway Schematic Entry, which enables the export of sub-circuits to Harmony-AMS simulator.

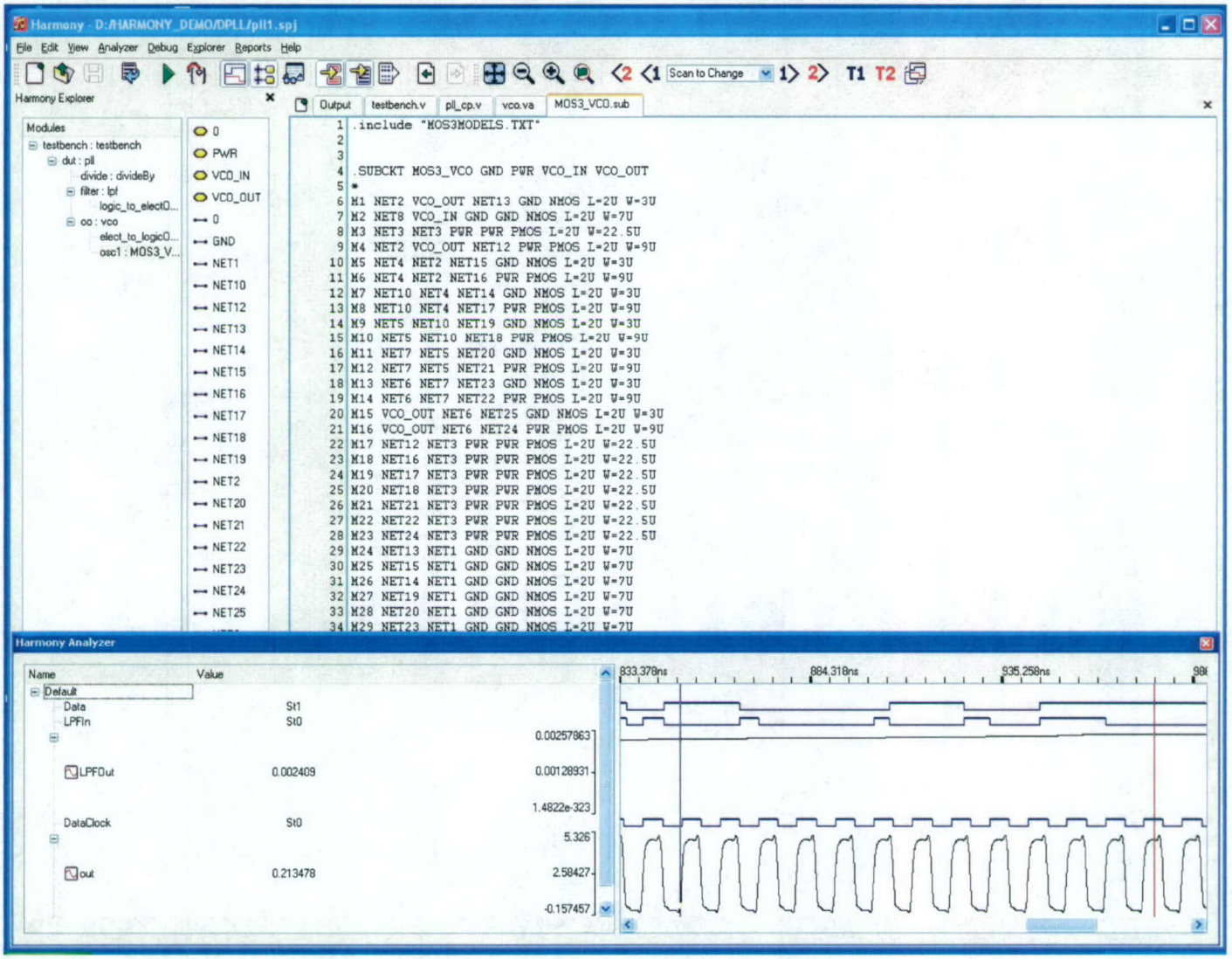

Figure 9: Harmony-AMS simulation of a Digital Phase Lock Loop (DPLL) as depicted in Figure 3.

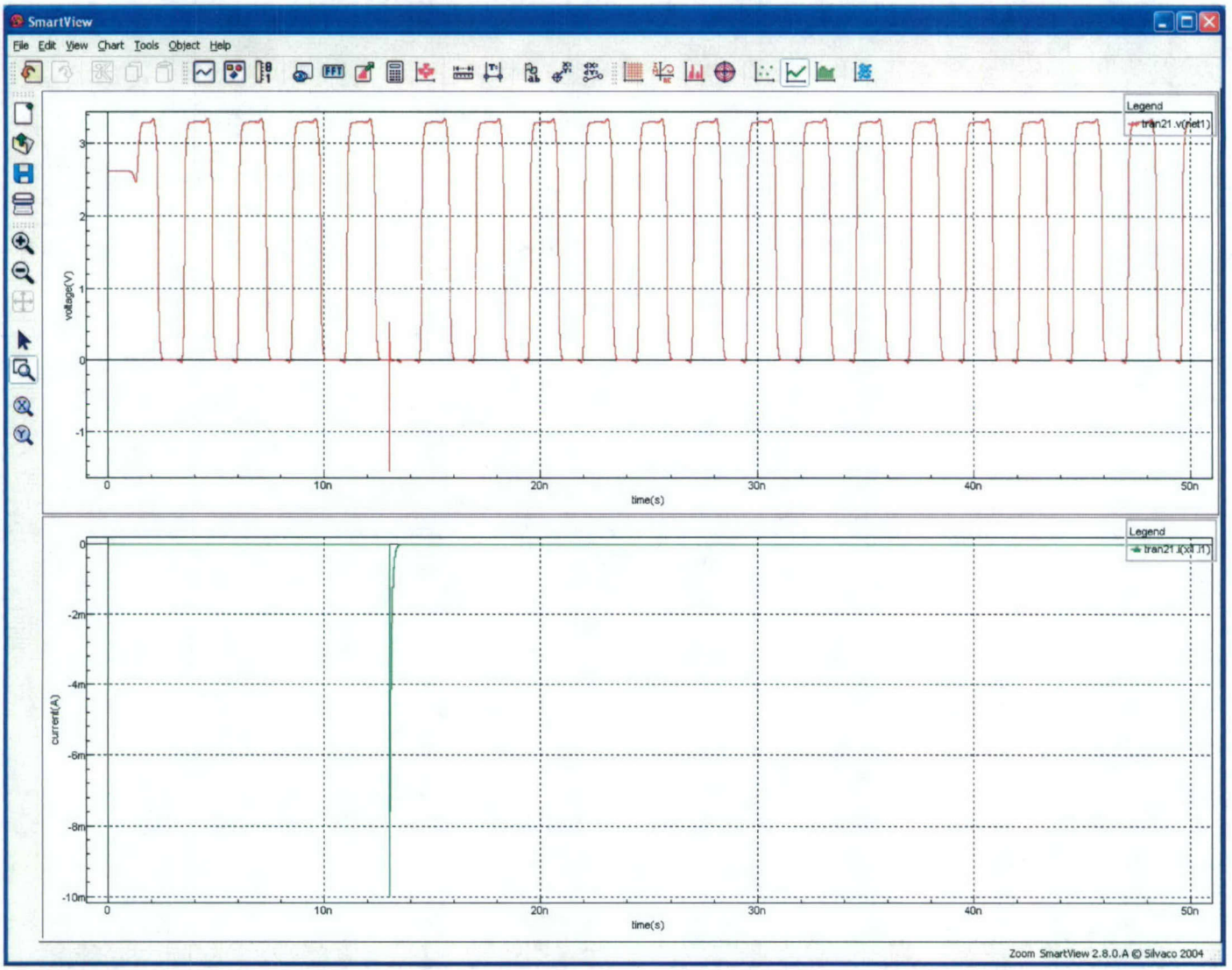

Figure 10: Output of Harmony-AMS from a Single Event Effects simulation at the VCO node of the DPLL simulation from Figure 9.

4.0 VALIDATION & SIMULATION RESULTS

Peregrine is experienced in both the design and manufacture of military electronics and their hardened by design experience is among the best. The development team worked closely with their engineering staff, led by Jim Swonger, to incorporate feedback on Harmony-AMS and more specifically on the radiation modeling capability. Peregrine identify a series of designs that they have already characterized for radiation response. These simulations were re-run in the Harmony-AMS simulator with the developed radiation models for comparison to the original measured data. This allowed Peregrine to perform Harmony-AMS simulations of previously designed and tested radiation hardened circuits. Feedback from this validation effort resulted improvements being made to the radiation physics within SmartSpice RadHard core device models.

The validation component also has ties to the integration with other EDA tool flows, as Harmony-AMS must have the capability to co-exist with other software packages. Peregrine Semiconductor, like most companies, has a multi-vendor tool flow in this case provided largely by Cadence. In parallel to the feedback provided on the test circuits and simulations Peregrine will verified that the Harmony-AMS's compliance to the Verilog-AMS standard from Acellera allowed for interoperability with their Cadence environment.

Our methodology for validation centered on the comparison of simulations to measured data as reported in published papers in recognized technical journals. This approach allowed us to validate our results over a broad spectrum of technologies including CMOS, Bipolar, Silicon on Insulator (SOI), Silicon on Sapphire (SOS), and SiGe. The scope of the Phase 1 effort did not permit a full manufacturing test, but based on our results we have a high degree of confidence in the validity of the simulation results. In this section we will start with one of the simulations we matched to published work for single event effects (SEE) in SiGe, secondly a combined environment simulation in which we added Total Ionizing Dose (TID) to the SiGe SEE simulations, and finally a Dose Rate (DR) simulation of an op-amp.

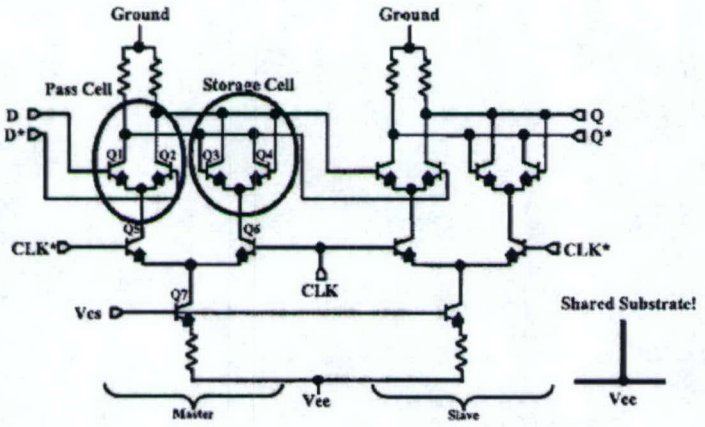

Fig. 3. Schematic of the rising edge-triggered master–slave D-flip-flop used in simulation. Each transistor element consists of five subtransistors arranged according to the CSH concept. The current source transistor Q7 was divided into five paths, with V_{cs1} controlling three paths and V_{cs2} and V_{cs3} controlling one path each. These paths were maintained separately through the clocking stage and through the pass and storage cells.

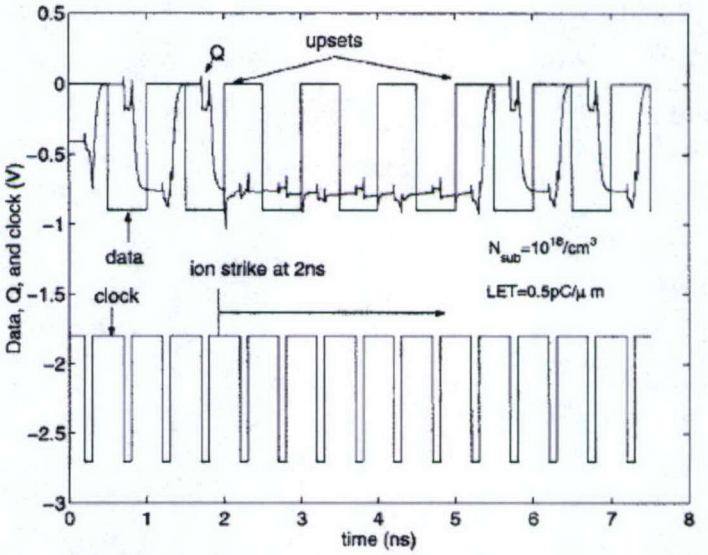

Fig. 5. Simulated SEE response of the D-flip-flop for $N_{sub} = 10^{18}/\text{cm}^3$ and LET $= 0.5$ pC/μm.

Reference :G. Niu, R. Krithivasan, J.D. Cressler, P. Marshall, C. Marshall, R. Reed, and D. Harame, Modeling of Single Event Effects in Circuit-Hardened High-Speed SiGe HBT Logic,IEEE Transactions on Nuclear Science, vol. 48, pp. 1849-1854, December 2001.

Figure 11: Our team was able to reproduce this published work within the Harmony-AMS with radiation enhancements.

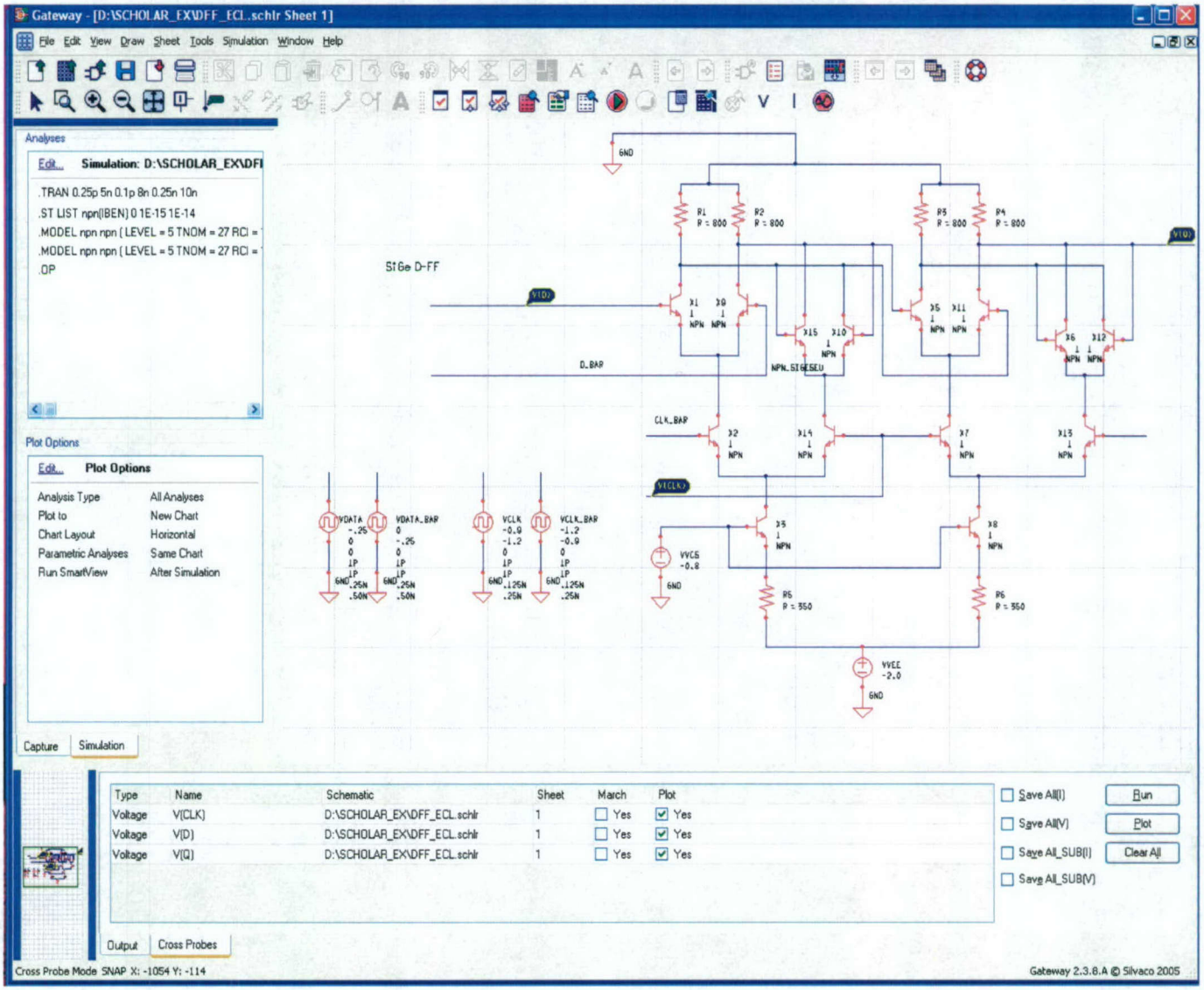

Figure 12: Schematic representation of a SiGe D Flip-Flop (see figure 11) which generates a netlist for simulation in Harmony-AMS.

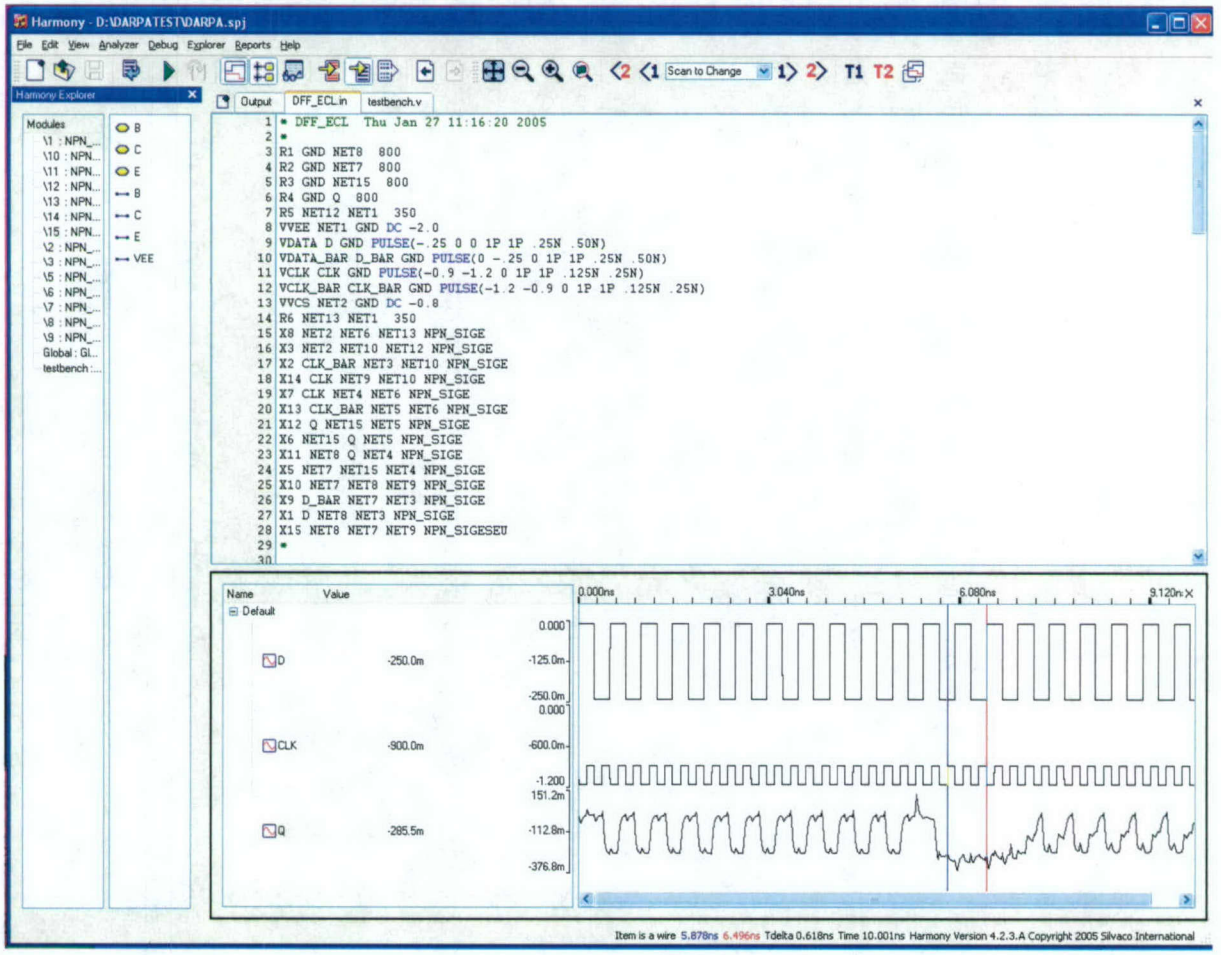

Figure 13: Harmony-AMS simulation of a SiGe D Flip-Flop with a Single Event Effect event with an LET of 20 (see figure 11).

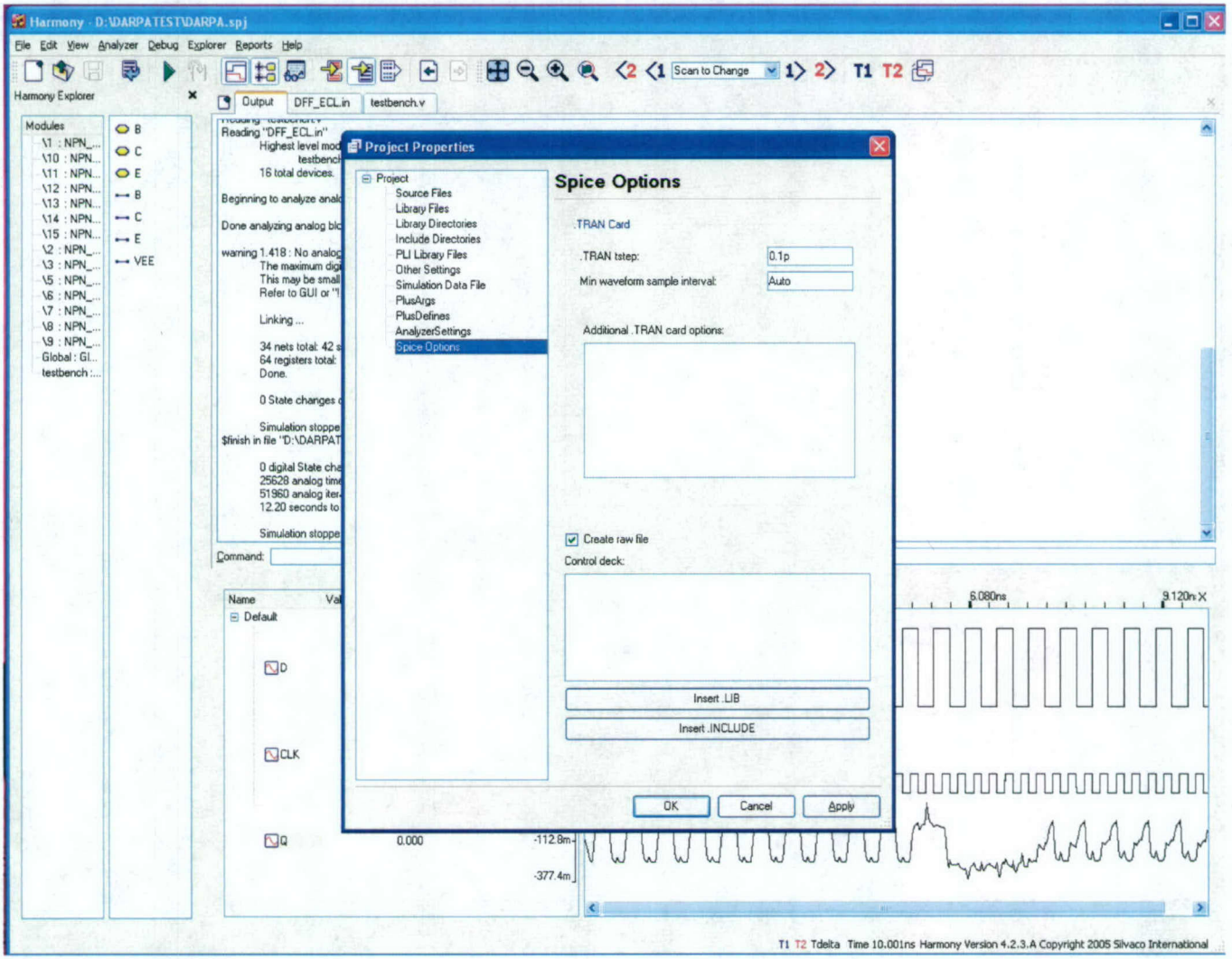

Figure 14: Output control panel in Harmony-AMS to display the waveforms generated by simulation in Silvaco's SmartView graphics viewer that enables advanced post-processing of signals.

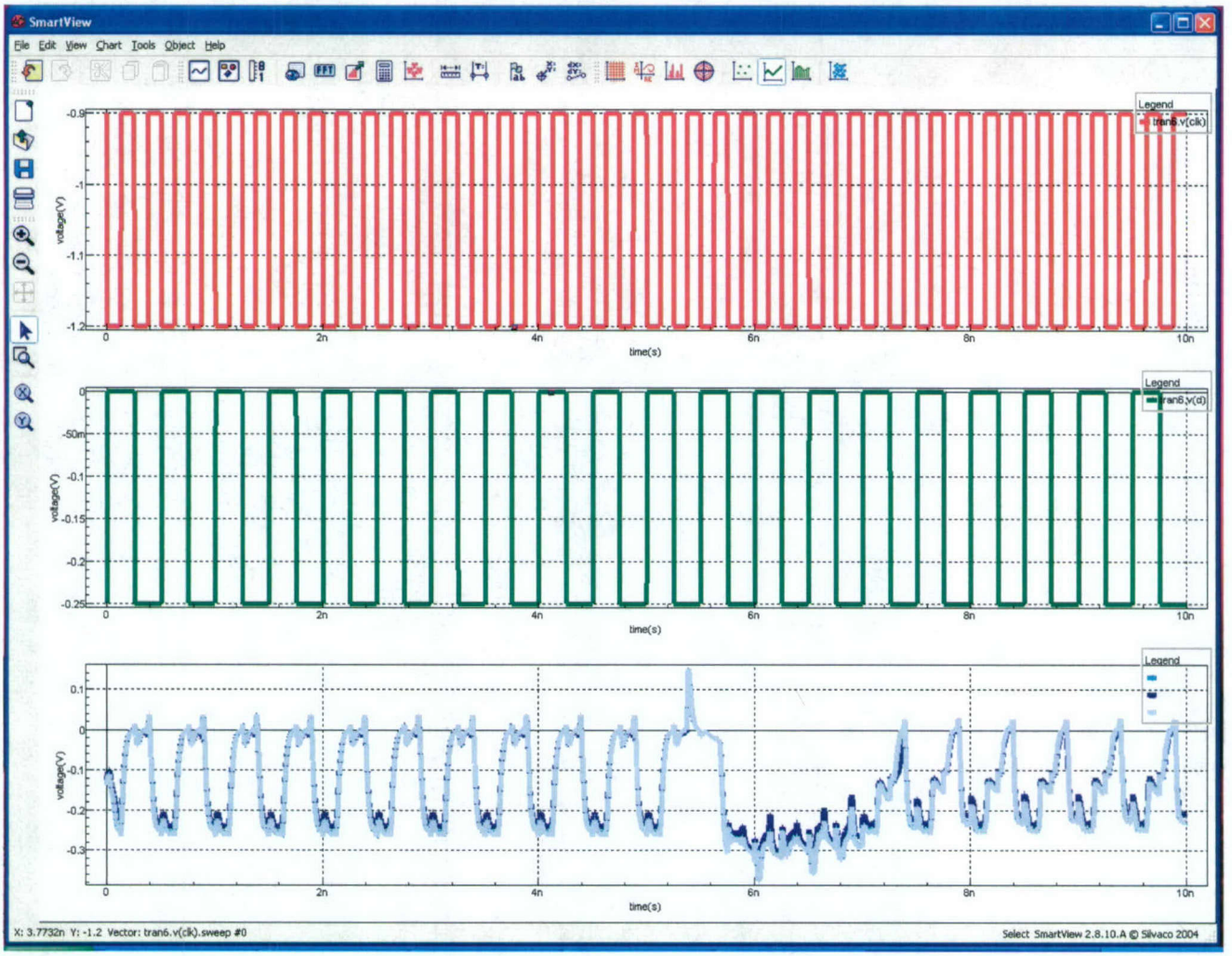

Figure 15: SmartView display of a combined environment (SEE & TID) simulation modeled in Harmony-AMS.

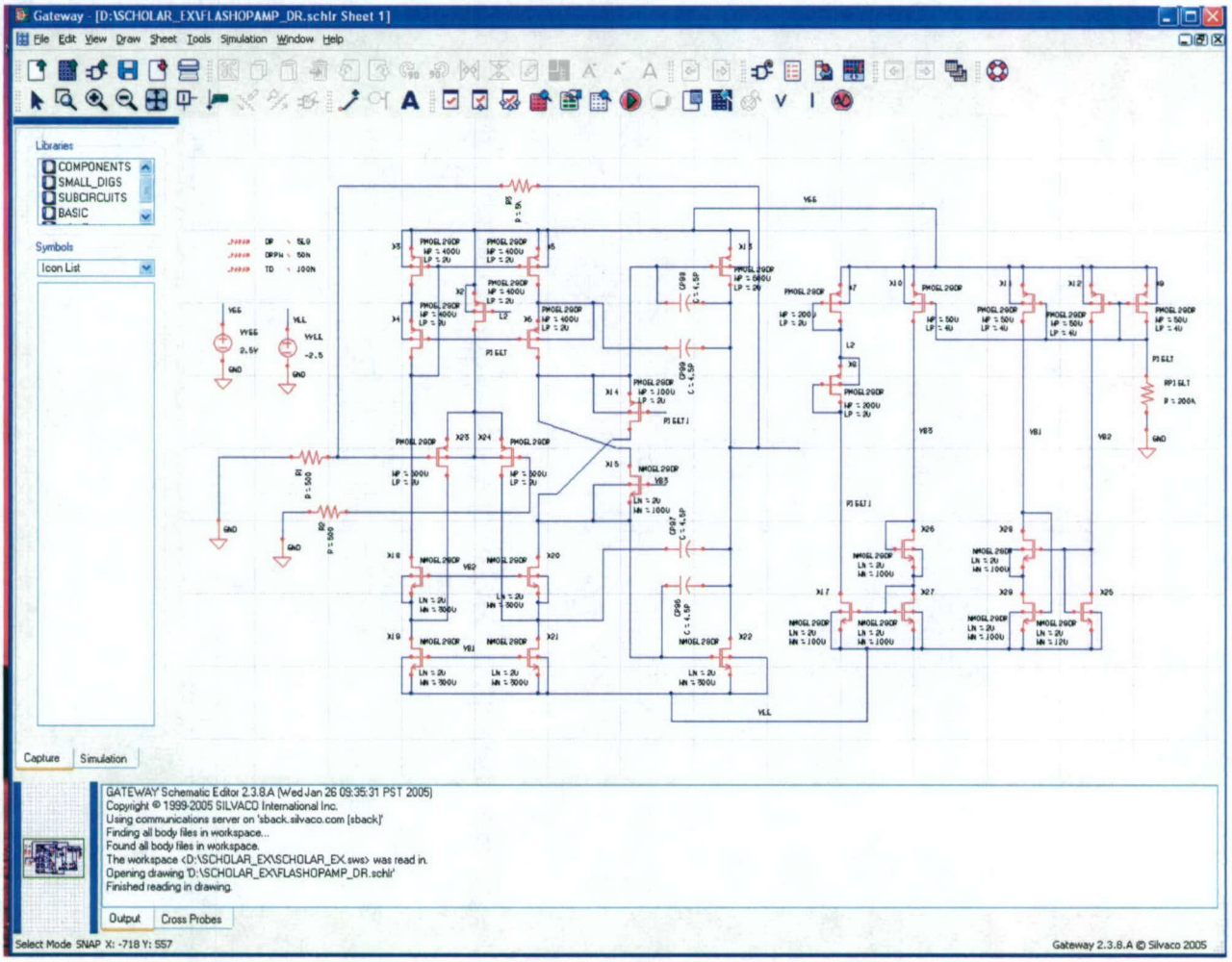

Figure 16: Schematic representation of a statically biased op-amp exposed to a dose rate pulse in a Harmony-AMS simulation

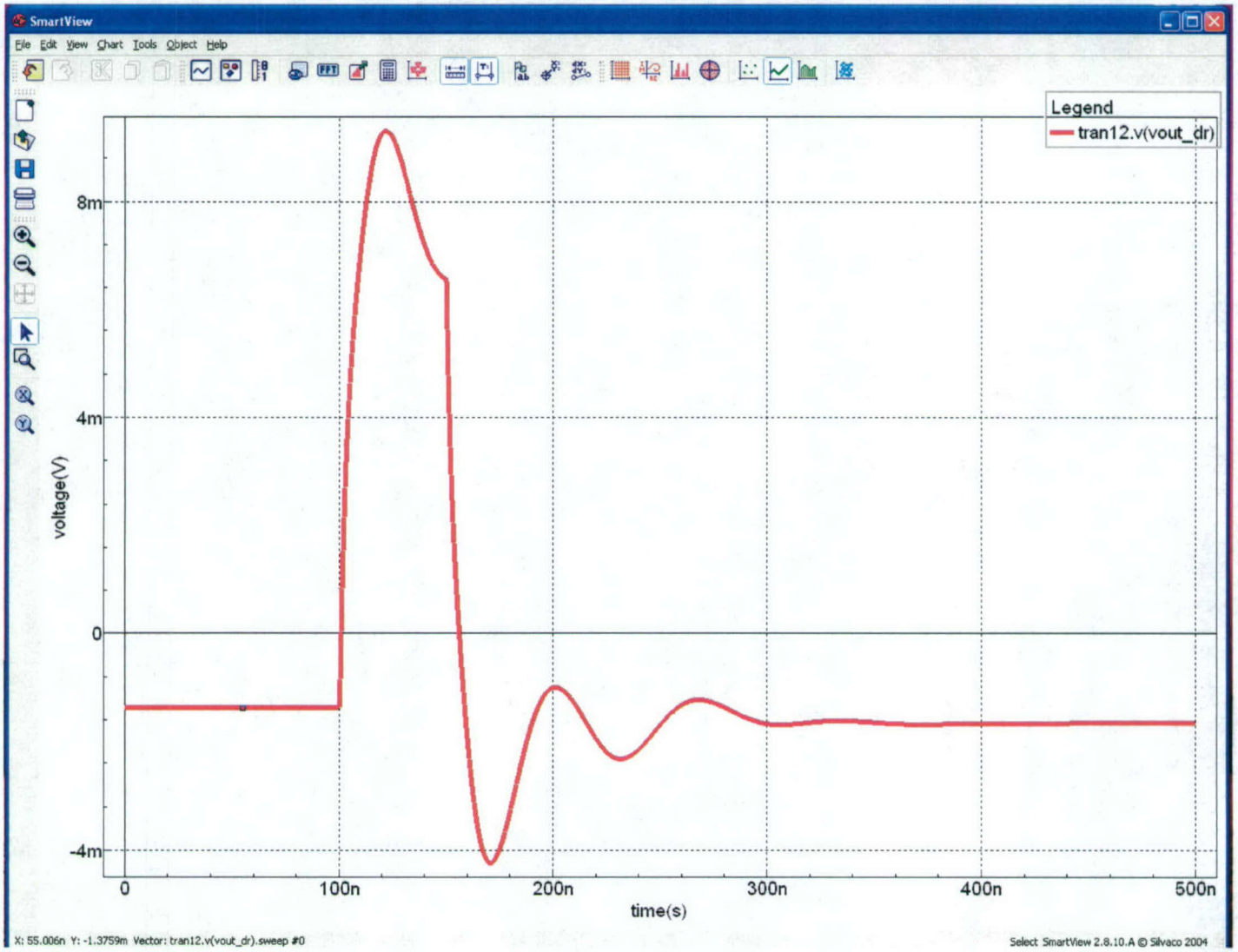

Figure 17: Dose Rate current pulse generated during mixed signal simulation displayed in SmartView.

5. SYSTEMS LEVEL INTERFACES

The Jaycor, San Diego office of Titan Corporation has provided system level perspectives on areas which are key to this effort:

1. Understanding Radiation Response Mechanisms
2. Design Hardening Techniques
3. Radiation Test and Characterization

Since its inception in 1975, the Jaycor team has combined these areas to develop approved test and evaluation protocols for verifying and validating radiation performance for DoD systems. The process by which this is used to develop and qualify radiation-hardened systems is illustrated in Figure 18.

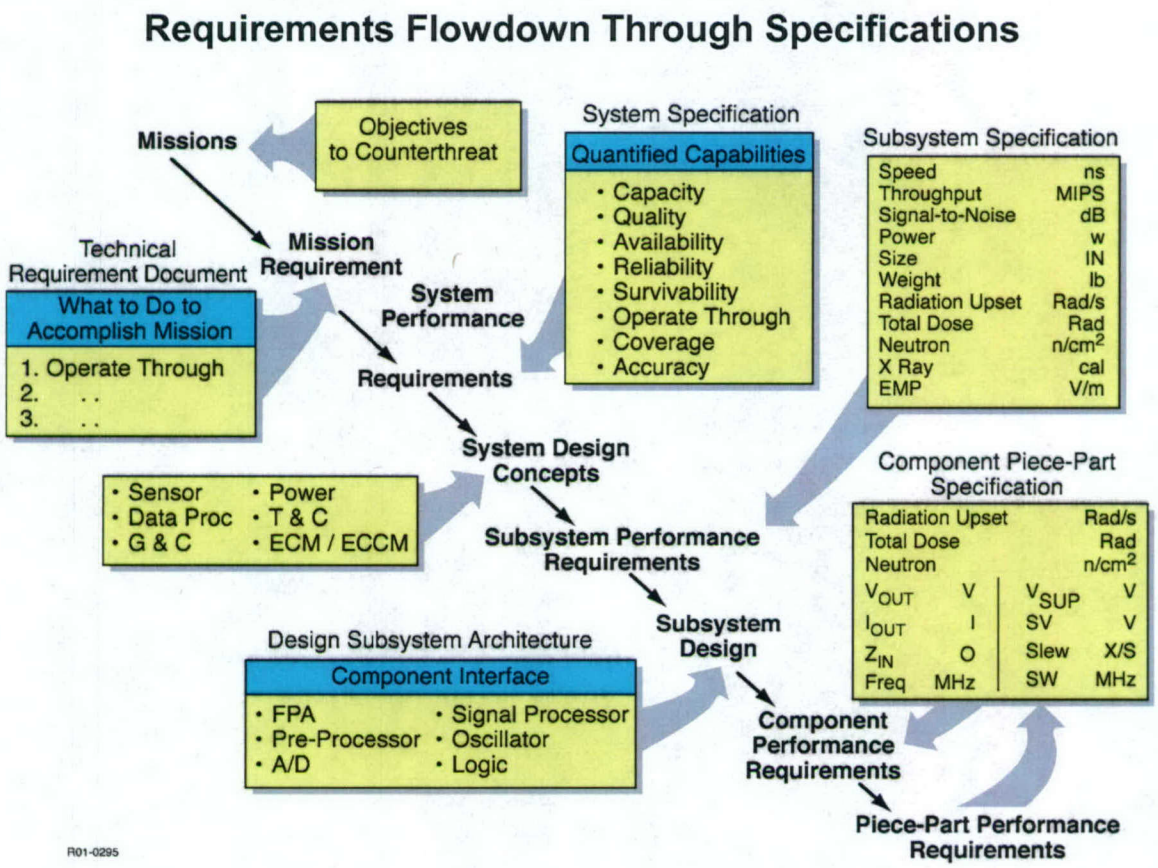

Figure 18: Top Down Approach connecting mission requirements to piece-part requirements.

There was a time when an industrial base of radiation hardened fabs/process technology and in-house design groups supplied the final component of this flow

down, the radiation hardened piece parts. Radiation hardness estimates could be made based on known hardness of a process technology and certified through radiation testing when necessary.

Times are different. In spite of government programs aiming at maintaining radiation hardened process technology, the DoD clearly has a need for design hardening methods and, more importantly, approaches to deploying these methods in ways that are (1) compatible with both the modern industrial base and (2) compatible with proven approaches to system hardening. The payoff in our Phase 1 effort is the realization of a methodology, depicted in Figure 18 that achieves both of these objectives.

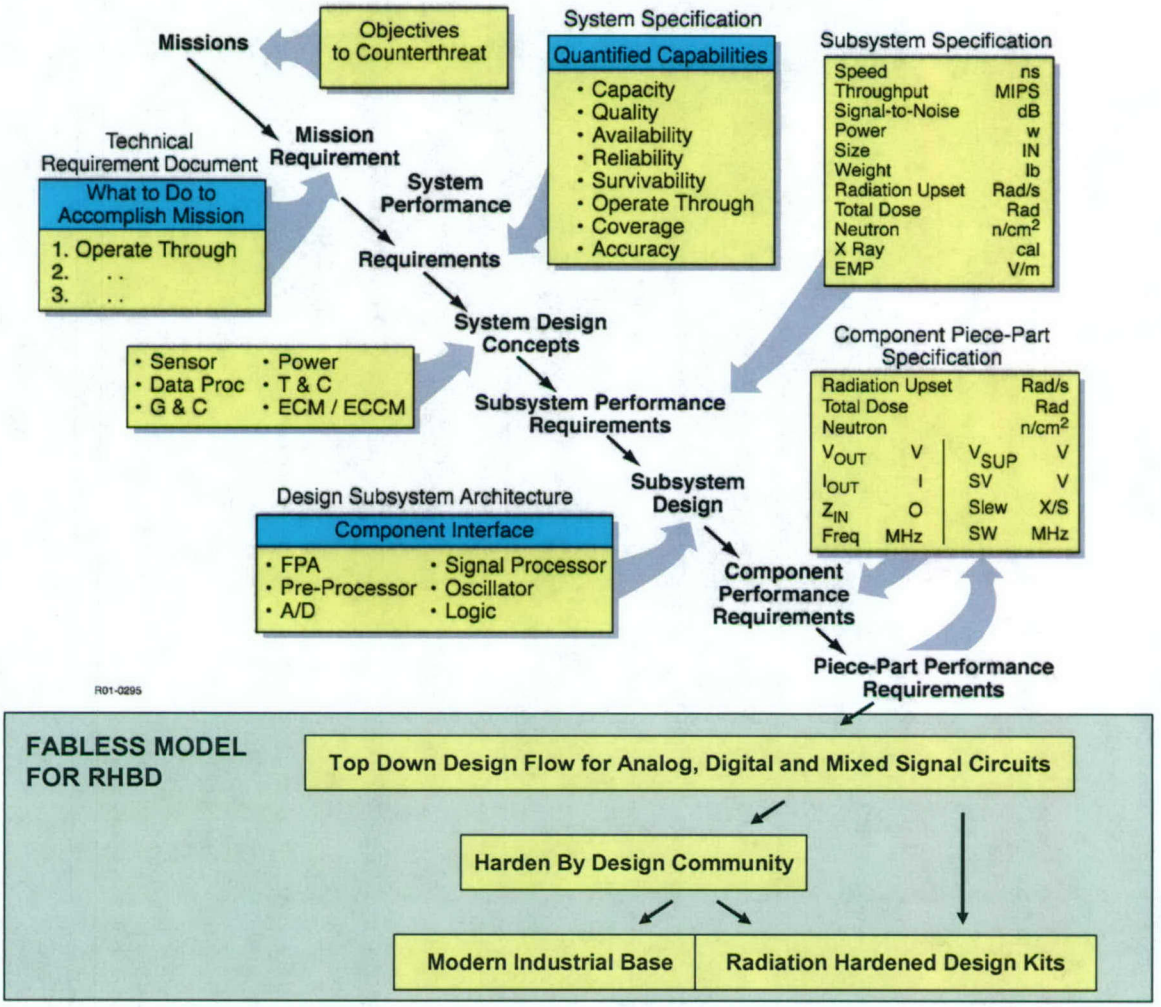

Figure 19: Extension of proven top down mission-to-piece part design flow to a fabless model for Radiation-Hardened By Design.

Figure 19 illustrates an exceptionally ambitious goal, however many of the components to achieve it exist.

- The original system hardening flow down as depicted in Figure 18 remains unchanged.
- Our DARPA Phase 1 effort resulted in a new simulator that is the "modeling-engine" at the heart of the Top Down Design Flow for Analog, Digital, and Mixed Signal Circuits.
- There is a growing Harden By Design Community with interest in foundry supported radiation hardened design flows
- There are ongoing efforts to develop radiation hardened design kits, which are the heart of a radhard design flow.

What has yet to be achieved is the application of this new radiation-aware modeling tool to develop complex DoD mission critical circuits, specifically circuits with sufficient radiation response characterization to be passed up to a traditional system hardening flow down process.

Our Phase 2 proposal to perform a harden by design analysis of a planned military GPS receiver product outlined an approach for exercising the most ambitious and unexplored aspects of Figure 19, specifically

- The creation of radiation aware design kit for Peregrine's 0.5 micron SOS process
- Radiation aware simulations of an inherently and unavoidably mixed signal (RF) system (Single Chip, Dual-band, Anti-jam GPS Receiver)
- Parametric studies of radiation response for developing hardness estimates for use in system level qualification
- Use results to estimate performance requirements for system level hardening for nuclear upset

Our Phase 1 funding obviously would not support such detailed simulation analysis, however we are continuing our efforts to secure funding to demonstrate the concepts of Figure 19. Titan involvement in these efforts is focused on taking the familiar role of developing approved test and evaluation protocols for verifying and validating radiation performance for DoD systems and enhancing it with *developing approved modeling and simulation protocols* for verifying and validation radiation performance.

5.1 FUTURE INTEGRATION POSSIBLE with OTHER SOFTWARE

Codes like ATR, C/LAMP, MCNP, HANE (High Altitude Nuclear Effects), ASSIST and DGBETS help define the characteristics of the nuclear radiation environments, i.e., X ray, gamma ray, neutron and electron ionizing dose, dose rate and fluence. When the characteristic radiation environments are defined, the next step is to transport these environments through various shielding materials to determine the amount of radiation allowable or tolerated within a given system. Codes that conduct shielding calculations are FSCATT, CEPHX/ONELD or CEPHX/ONEBFP, PHOTOCOEF and DEPOSIT. Other codes such as MCNP and BOXIEMP I and II or JaySIM do provide similar calculations plus other additional radiation effects simulations, such as IEMP (internal package electromagnetic pulse effects) or cable SGEMP effects.

On the materials and structure side, transport modeling is not the only type calculation, but also codes like PUFF-TFT, BUCKL and LS-DYNA3D can predict the effects from thermal mechanical and response effects, like heating and spallation. When the radiation spectra are determined inside a package, this information is now used in circuit simulators to model the circuit response at the IC or board level. Such effects include (1) large photocurrents, (2) gain degradation from displacement damage or (3) threshold voltage shifts from total ionizing dose. Codes like RHTCAD, SmartSpice RadHard, ChileSPICE, and Xyce provide that service.

As evident in Figure 15, there are important roles for circuit response simulation. Prior efforts on radiation hardened systems design have recognized the need for SPICE simulation and also identified RHTCAD as a useful element of radiation hardened design. As such, systems design represents an important platform in which the DARPA supported effort in radiation aware EDA tools can be deployed in military systems design activity.

A mixed signal design tool with radiation response capability enables systems level design optimization. In this framework the parameters can are all subject to system level requirements that flow down to lower levels in the architecture of a design. Silvaco's radiation enhancements to the HARMONY-AMS and SmartSpice tools will provide a significant improvement to prior capability. For example, it will connect systems analysis to the earliest stages of the design cycle, in particular, design using commercial foundries. This will create a hardened by design capability at the part level operating within a system level process for RHBD. Tradeoffs for shielding, orbit, board and packing can be made along with circuit level tradeoffs made within the HARMONY-AMS flow.

6. INTEGRATION INTO OTHER EDA TOOL FLOWS

The Harmony-AMS product is a central piece of the analog/mixed signal tool flow offered by Silvaco. Like many of our other tools Harmony-AMS maintains industry standard interfaces for interoperability. The simulator can take IEEE-1364 Verilog HDL, Verilog-A, Accellera Verilog-AMS, and Berkeley SPICE netlists. The last is of particular importance, as nearly any foundry in the world will either provide a SmartSpice or HSPICE foundry supported model inside their design kits. SmartSpice is HSPICE compatible meaning that it will read and accept HSPICE models, syntax, and statements. This compatibility allows Harmony-AMS to accept HSPICE model files and syntax with very little or no input from the user.

The two key elements in tool interoperability are the inputs into the tool and equally as important the outputs.

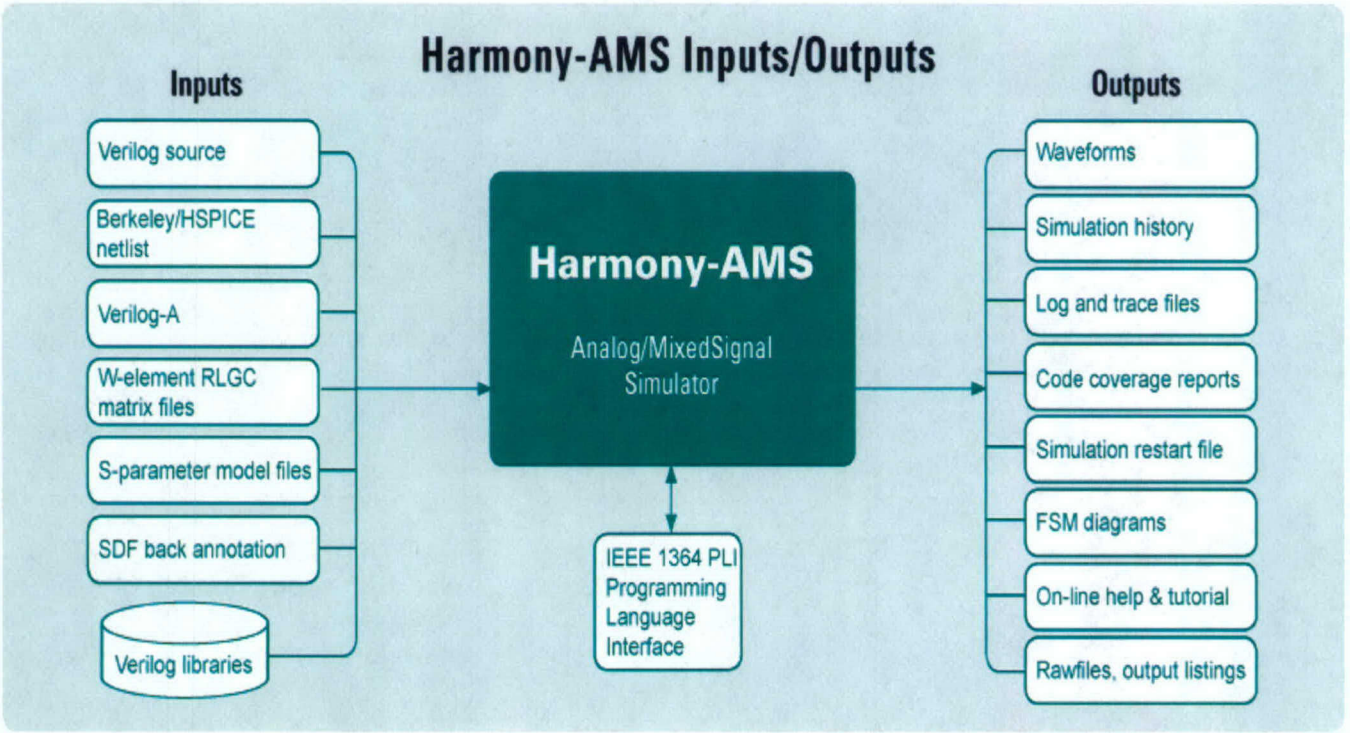

Figure 20: Harmony-AMS Inputs/Outputs

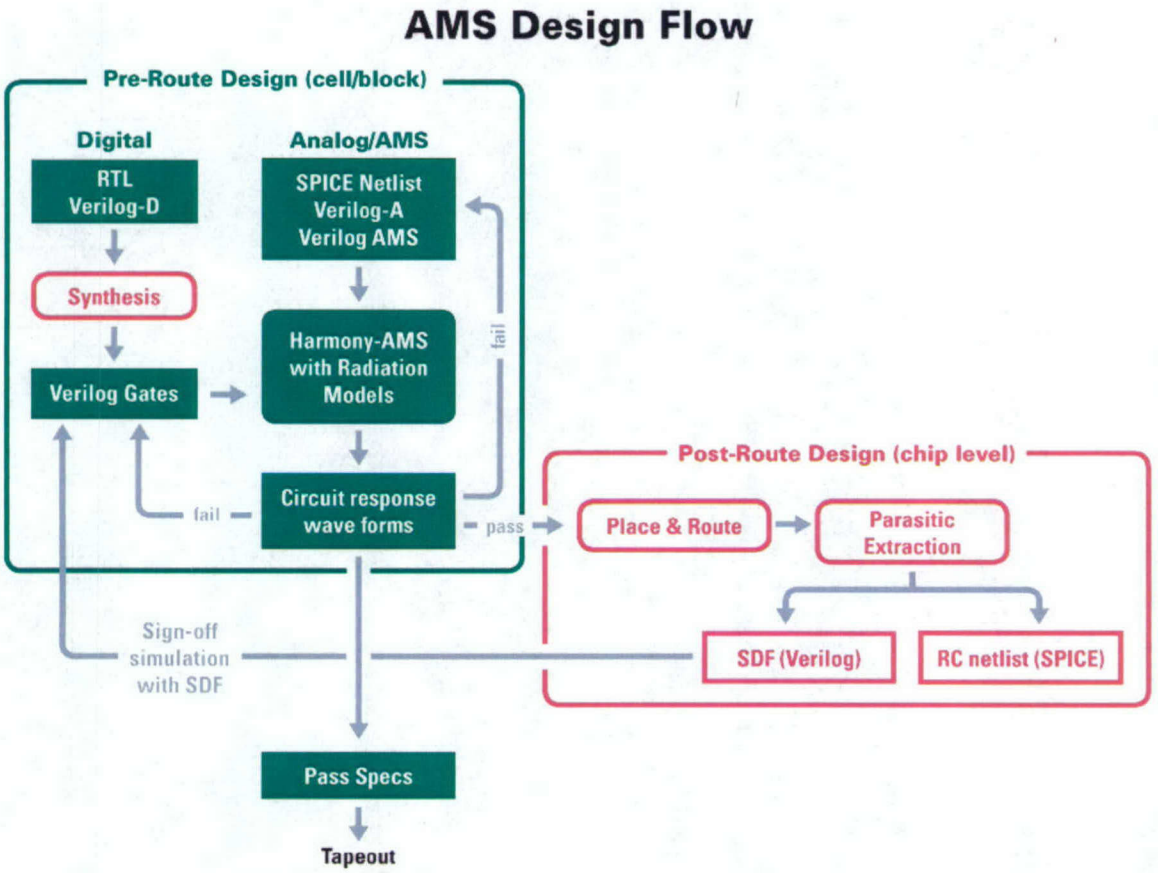

Figure 21: Analog/Mixed Signal (AMS) Design Flow

Our efforts to make the commercial version of Harmony-AMS compatible with other EDA tool flows carries over to the radiation knowledgeable product as well. Harmony-AMS will simulate and display results based on a number of various industry standard inputs (IEEE 1364-2001 Verilog HDL, Accellera 2.2 standard for Verilog-AMS and Verilog-A, Berkeley SPICE netlists, HSPICE netlists, and SmartSpice netlists) with no modification.

The output, Figure 20, enables the user to determine if the results are satisfactory or if additional design work is required; if this is the case the modifications are done in other tools that generate these inputs. Once a satisfactory result is obtained the corresponding SPICE netlists and Verilog code are passed to a full chip place & route tool. When the final chip layout is generated the RC data for this layout must be extracted to reflect the new structures created by the router. The output of this extraction is a back-annotated SPICE netlist for the Analog blocks, and a Standard Delay Format (SDF) file for the Digital and Mixed Signal elements. Harmony-AMS reads SDF files as input and the final pass of simulation occurs when Harmony-AMS re-simulates the original 'pass' design with this new SDF information. If the simulation still meets requirements the loop is complete and the design is ready

for tape-out; however if the result is unacceptable changes must be made either at the place and route level or the initial design before Harmony-AMS simulation.

7.0 SUMMARY

We successfully completed our Phase 1 objectives during our period of performance and the team was pleased with the results. Unfortunately, our effort was not selected for funding for a Phase 2 award. We had hoped to embark on an effort to fully validate the Harmony-AMS product in a Radiation Hardening By Design (RHBD) tool flow, manufacture a test design, and finally compare measured data after radiation testing to our simulations. While this did delay our progress we have found a eager commercial market for the SEE and combined environment simulation capability, and we are pleased to report that Silvaco will release a radiation aware version of it's Harmony-AMS product in the first quarter of 2005. One of the stated goals of the SBIR program is to bring novel ideas and critical technology from conception to commercialization, and in this case we were able to accomplish this in six months.

The value of Titan and Peregrine can not be overstated- Silvaco's developers were able to get invaluable real time feedback from chip designers, manufacturing teams, and the perspective of systems engineering. This kind of coordination not only speeds a product to market, but also reduces the risk that our target customer base will not adopt the new software package. The growing commercial customer base for Harmony-AMS also ensures the continued development and improvement of the software which in turn will allow those with access to the radiation enhanced version of the product to leverage the most recent developments driven by the commercial customers.

We would also like to take this opportunity to thank the DARPA program office and specifically Dr. Krishnan for his support. The rapid commercialization of this software would not have been possible if not for the financial support to enable our team to spend quality engineering time together.

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6. AUTHOR(S)
Christopher Nicklaw
Mark Maurer
Chuck Tabbert
Randall Milanowski

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Silvaco Data Systems
4701 Patrick Henry Drive
Building #2
Santa Clara, CA 95054

The Titan Corporation
3394 Carmel Mountain Road
San Diego, CA 92121

Peregrine Semiconductor
2921 Carlisle Ave NE Suite 200K
Albuquerque, NM 87110

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Defense Advanced Research Projects Agency
ATTN: MTO (Dr. Anantha Krishnan, Sponsor)
3701 North Fairfax Drive
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This report covers the final report of our phase I effort to develop a mixed signal simulator with radiation modeling capability. Silvaco's Harmony-AMS (Analog/Mixed Signal) simulator was modified to enable the simulation of singl event effects, total ionizing dose, and dose rate in a commercial hierarchical design flow.

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